Design of Novel Architectures and FPGA Implementation of 2D Gaussian Surround Function

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A new design and novel architecture suitable for FPGA/ASIC implementation of a 2D Gaussian surround function for image processing application is presented in this paper. The proposed scheme results in enormous savings of memory normally required for 2D Gaussian function implementation. In the present work, the Gaussian symmetric characteristics which quickly falls off toward plus/minus infinity has been used in order to save the memory. The 2D Gaussian function implementation is presented for use in applications such as image enhancement, smoothing, edge detection and filtering etc. The FPGA implementation of the proposed 2D Gaussian function is capable of processing (blurring, smoothing, and convolution) high resolution color pictures of size upto 1600 × 1200 pixels at the real time video rate of 30 frames/sec. The Gaussian design exploited here has been used in the core part of retinex based color image enhancement. Therefore, the design presented produces Gaussian output with three different scales, namely, 16, 64 and 128. The design was coded in Verilog, a popular hardware design language used in industries, conforming to RTL coding guidelines and fits onto a single chip with a gate count utilization of 89,213 gates. Experimental results presented confirms that the proposed method offers a new approach for development of large sized Gaussian pyramid while reducing the on-chip memory utilization.

Keywords : FPGA, Gaussian Surround Function, Hardware Architecture, Verilog.

1. INTRODUCTION

With the widespread use of technologies like digital television, internet streaming video and DVD video, Gaussian function has become an inevitable component of image/video processing [1] and pattern recognition. Hardware realization of 2D Gaussian surround function for image processing applications demands huge on-chip memory requirement, with massive computations. Further, these functions might not fit on a single FPGA device. This is due to the reason that Gaussian function has an exponential distribution with maximum entropy and implementation such functions using software schemes are complex from computation point of view. In addition, Gaussian function is a non-causal, which implies that function is symmetric about the origin in time domain. Gaussian filter implementation with smaller kernel size in order to blur an image have been reported by number of researchers [2]. However, design of Gaussian function for large kernel size requires enormous amount of resources on FPGA with incredible raise in the total equivalent gate count.

The new approach for 2D Gaussian function design provides a technical solution appropriate for the broad range of applications, from image pre-processing to pattern recognition. It simplifies the computational complexity with considerable saving in the memory requirement. The work proposed here utilizes the symmetry property of Gaussian surround function in order to save hardware resource, particularly memory requirement on FPGA. The technical design presented in this work is highly focused on providing huge throughput to process images as well as motion pictures. The Gaussian surround function is designed to process high quality images with picture size ex-
REFERENCES


Table 4
Design Mapped on Various FPGA Devices

<table>
<thead>
<tr>
<th>Device</th>
<th>LUTs</th>
<th>Gates</th>
<th>Utilization</th>
<th>Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>XC2S50-6TQ144</td>
<td>825 out of 1536</td>
<td>62,455</td>
<td>53%</td>
<td>61.992 MHz</td>
</tr>
<tr>
<td>XC2S200-6PQ208</td>
<td>825 out of 4704</td>
<td>62,455</td>
<td>17%</td>
<td>61.992 MHz</td>
</tr>
<tr>
<td>XC3S1600E-5FG484</td>
<td>825 out of 29504</td>
<td>89,213</td>
<td>5%</td>
<td>160.458 MHz</td>
</tr>
<tr>
<td>XC2VP40-7FG676</td>
<td>825 out of 38784</td>
<td>89,213</td>
<td>2%</td>
<td>223.04 MHz</td>
</tr>
</tbody>
</table>


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